A Monolithic 60 GHz Diode Mixer and IF Amplifier in Compatible Technology

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Abstract —**To integrate key components of a millimeter-wave system monolithically in the future a novel technology has been developed which allows the integration of Schottky diodes and MESFET's on one chip. The fabricated Schottky diodes have a cutoff frequency f_T of 2300 GHz. A monolithic 60 GHz mixer chip with these diodes shows a conversion loss of 6 dB and a noise figure (DSB) of 3.3 dB. The MESFET's, have an f_{max} up to 70 GHz. A realized two-stage IF amplifier shows a gain of 20.6 dB and a noise figure of 1.7 dB at 4 GHz.**

I. Introduction

The LOW-COST, high-volume production of millimeter-wave systems relies on the availability of millimeter-wave MMIC's. During the past few years great efforts have been made to push the frequency limits of the necessary key components to higher frequencies [1]–[3]. In addition, technologies which allow the integration of different circuit functions in a monolithic way will be of great advantage [4], [5]. On the basis of earlier results [6], [7], a new technology has been developed which allows the integration of Schottky diodes ($f_T = 2300$ GHz), varactor diodes, and MESFET's ($f_{max} = 70$ GHz) on the same chip. With this technology it is possible to integrate diode mixers, IF amplifiers, and local oscillators—the key components of a receiver front end—on one chip. This paper describes the design and fabrication of a 60 GHz mixer and a two-stage IF amplifier.

II. Technology

A novel technology for the monolithic integration of both planar Schottky mixer diodes and GaAs MESFET's has been developed and used for the fabrication of these circuits. The processing sequence is based on an earlier technology which was applied to circuits operating at lower signal frequencies and lower IF frequencies [6]. That technology differed from most other MMIC technologies in that it incorporated an n^+ buried layer to reduce the series resistance of the Schottky mixer diodes. For the present work IF frequencies of up to 5 GHz were envisaged and the integration with further stages, such as the local oscillator, should be possible. For this reason, recessed gate MESFET's with electron beam lithography of the gate structures were included.

Manuscript received May 3, 1989; revised July 28, 1989.
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IEEE Log Number 8931093.

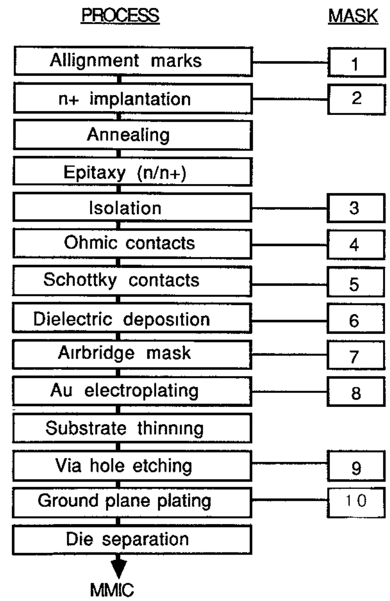

Fig. 1. Processing sequence for millimeter-wave GaAs MMIC's.

The processing sequence, requiring a total of ten masks, is illustrated in Fig. 1. All the lithographic processes apart from that for the gate metallization are carried out using standard contact lithography. A schematic cross section of the completed active devices is shown in Fig. 2.

The buried n^+ zones were formed by selective implantation of Si^+ and Si^{++} into the semi-insulating substrate using SiO_2 as a mask. A series of implantation energies of up to 360 keV were used to obtain a flat profile for the as-implanted ions. The sheet resistance of the n^+ buried layer is an important parameter limiting the series resistance and hence the high-frequency properties of the Schottky diodes. This sheet resistance was optimized by varying the implantation parameters, the annealing procedure, and the composition of the capping material used for

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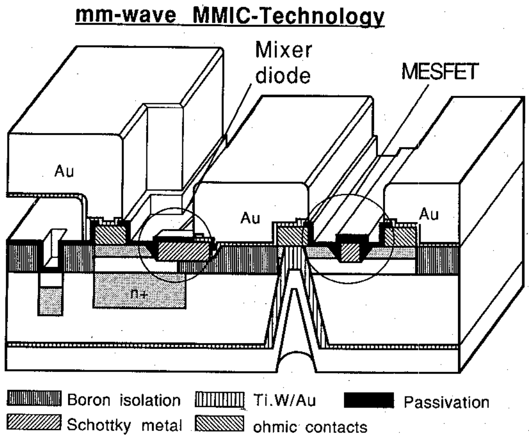

Fig. 2. A schematic cross section of the active devices.

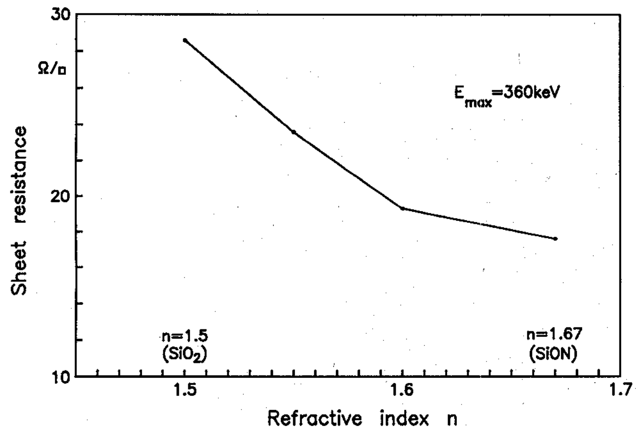

Fig. 3. Sheet resistance of the n^+ buried layer as a function of the refractive index of the SiON capping layer.

the subsequent rapid thermal anneal (RTA) of the implanted substrate. The optimization of the annealing cycle resulted in annealing parameters of 1050°C for 5 s [8] for the annealing system which was used (AG Associates, Heatpulse). During annealing the substrates were coated on both sides of the wafer to prevent evaporation from the GaAs surface.

The properties of the capping material strongly affect the sheet resistance of the resulting n^+ layer. Fig. 3 shows measured sheet resistance as a function of the refractive index of the SiON capping layer. The refractive index was varied between 1.5, corresponding to SiO_2, and 1.67. For refractive indexes higher than 1.67, corresponding to higher N content, the annealing resulted in degradation of the capping layer and the GaAs surface. The variation in sheet resistance is more than a factor of 2. Best results were approximately 17 Ω/sq., and values lower than 20 Ω/sq. could be routinely obtained. A depth profile measured using an electrochemical profiler is shown in Fig. 4. The high levels of activation leading to maximum carrier concentration of 5×10^{18} cm^{-3} could only be obtained by RTA. For furnace annealing a saturation of the maximum carrier concentration at approximately 2×10^{18} cm^{-3} was observed.

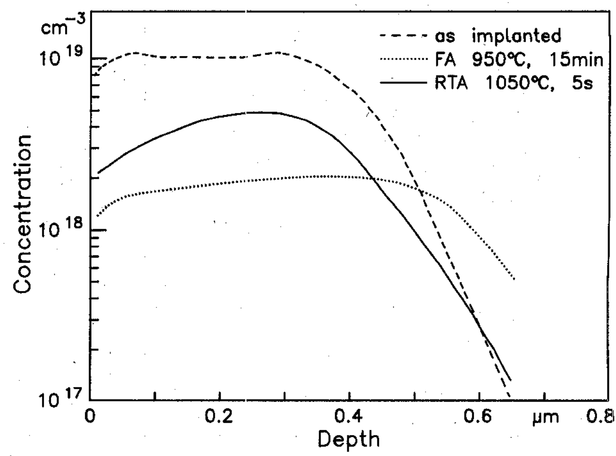

Fig. 4. A measured carrier concentration profile of the implanted n^+ zones after annealing.

After suitable surface preparation, the active n layer ($d = 0.2$ μm, $n = 3.5\times10^{17}$ cm^{-3}) and a further n^+ layer ($d = 0.1$ μm, $n = 2\times10^{18}$ cm^{-3}) were deposited by MOCVD in a horizontal reactor operating at atmospheric pressure. This active layer is used for both the MESFET devices and the mixer diodes so that the carrier concentration of the material for the Schottky diodes is higher than that usually used for this application. In the areas between the active devices these epitaxial layers were subsequently made highly resistive by selective boron implantation. Apart from the gate recessing, the GaAs surface remains completely planar. AuGe ohmic contacts were fabricated using a suitable lift-off procedure and RTA alloying. Ohmic contact resistances were typically 1×10^{-6} Ω cm^{-2}.

In the areas between the active devices these epitaxial layers were subsequently made highly resistive by selective boron implantation. A multiple implantation with energies between 30 and 120 keV and a total dose of 1.9×10^{12} cm^{-2} were implemented. The doses and energies were selected to give a flat profile with an implanted ion concentration of approximately 5×10^{16} cm^{-3} over the 0.3-μm-thick epitaxial layers. After implantation and alloying of AuGe ohmic contacts, the sheet resistance of the epitaxial layers was approximately 10^9 Ω/sq., corresponding to a specific resistivity of 3×10^4 Ω·cm. This material provides more than adequate isolation of the devices.

The Schottky contacts for the MESFET gates and the Schottky diode fingers were defined by electron lithography using Cambridge EBMF 10.5 equipment. A single 0.7-μm-thick layer PMMA resist process was applied [9]. The exposure conditions were optimized to give undercut resist profiles suitable for lift-off processing. The gate structures were aligned to the source and drain contacts using alignment marks fabricated with the AuGe metallization.

An alignment accuracy of ±0.1 μm could be obtained. After wet chemical recess etching, the contacts were formed by evaporation of Ti Pt Au and lift-off. Both the MESFET's and the diodes are recessed simultaneously. A minimum structure size of 0.3 μm for the 0.4-μm-thick gate metallization was obtained. All the devices were passivated

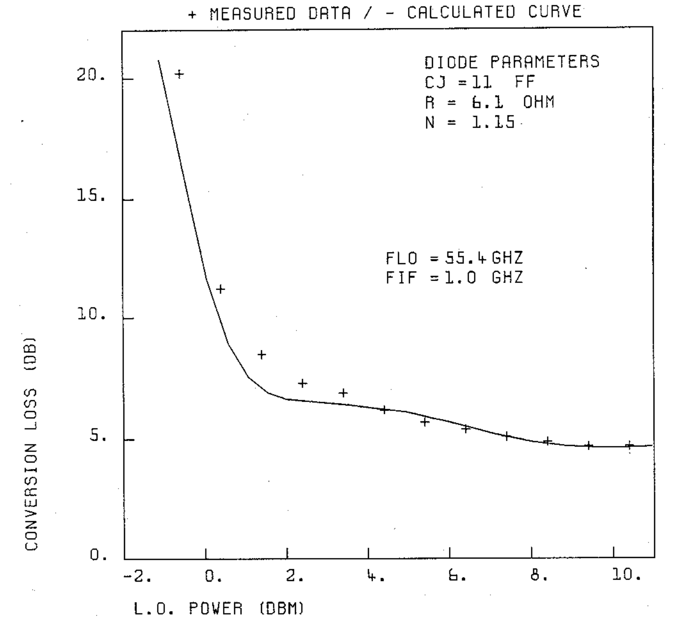

Fig. 5. Measured and calculated conversion loss of a Schottky mixer diode.

by a plasma-deposited Si_3N_4 layer, avoiding surface damage which could degrade the performance of the devices. The Si_3N_4 was also used for the insulator in the MIM overlay capacitors. The technology includes the fabrication of both air bridges for low-capacitance crossovers and via holes for low-inductance ground connection.

III. Diodes and MESFET's

A model of the Schottky diode has been developed. The technological parameters and the diode structure are taken into account for the determination of the series resistance and the junction and parasitic capacitances.

The diode model is used in a CAD mixer analysis program based on a harmonic balance technique [10], [11]. It is assumed that the RF excitation is negligibly small compared to the LO so the large-signal analysis is performed under LO excitation only. The time waveforms of the junction capacitance and conductance of the diode are deduced. The Fourier series coefficients are calculated for the mixing frequencies, and the conversion matrix of the mixer is derived.

Fig. 5 shows, for example, a comparison of measured and calculated conversion loss of a single diode versus LO power. This diode has three fingers, each 0.3×4 μm^2, and is shown in Fig. 6. The values of the junction capacitance and the series resistance are respectively 11 fF and 6.1 Ω and result in a cutoff frequency of 2370 GHz. For this measurement the diode is mounted in a special test fixture and the IF port is matched.

The fabricated MESFET's have gate lengths between 0.3 and 1.0 μm and different gate widths in π and multifinger configurations to satisfy the different requirements of the different parts of the receiver circuit. The short-gate-length transistors, for example Fig. 7, will be used for an integrated LO, consisting of a 27.7 GHz FET oscillator and a 27.7 GHz amplifier. Together with the Schottky mixer diodes, varactor diodes are with this technology under development to realize a varactor diode doubler to obtain 55.4 GHz LO.

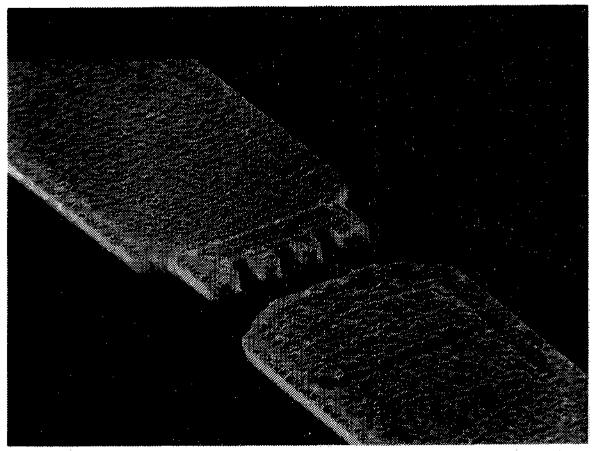

Fig. 6. A three-finger Schottky diode.

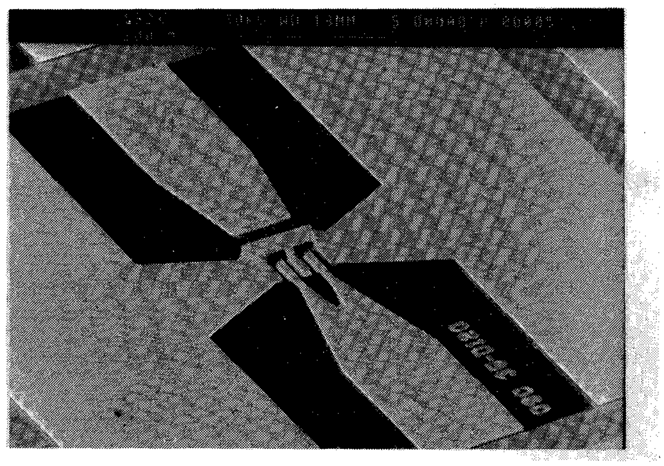

Fig. 7. A four-finger MESFET.

S-parameter measurements of the transistors showed an extrapolated $f_{max} = 70$ GHz and a $MAG = 7$ dB at 30 GHz. The transistors with longer gate lengths (0.75 μm) were used for the design of an integrated low-noise IF amplifier with two stages for an IF bandwith from 4 to 5 GHz. Noise figures of 0.8 dB at 4.5 GHz with an associated gain of 11 dB have been measured.

IV. 60 GHz Mixer

The mixer analysis is performed with the software described in the previous section. To obtain good performances the RF, LO, and image frequency impedances are optimized. In the millimeter-wave range, it is particularly important to minimize the demand for LO power.

The developed single balanced mixer chip is shown in Fig. 8. The chip thickness was chosen to be 150 μm. To avoid problems with coupling effects and microstrip (MSL) discontinuities and to get optimum design possibilities, an impedance level of 70 Ω was chosen. The in-house software has been improved to calculate MSL discontinuities and radial stubs for the millimeter-wave frequency range

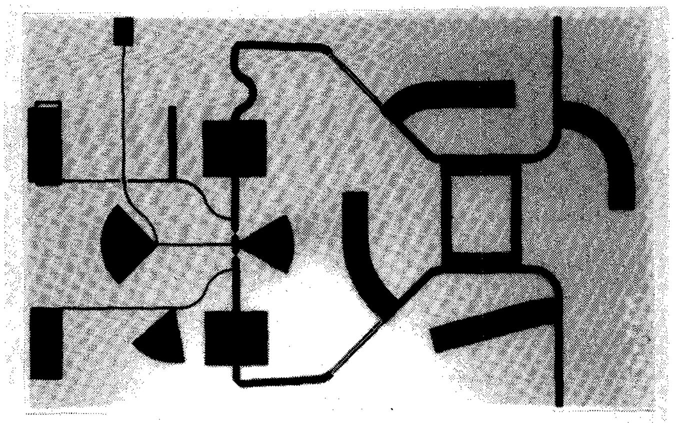

Fig. 8. 60 GHz mixer chip.

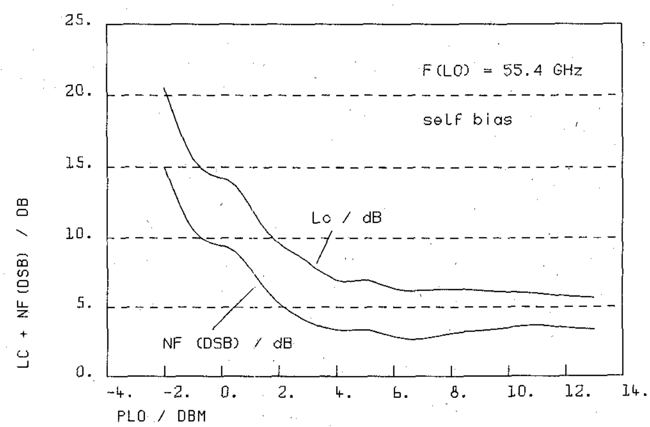

Fig. 10. Conversion loss and noise figure of the mixer chip.

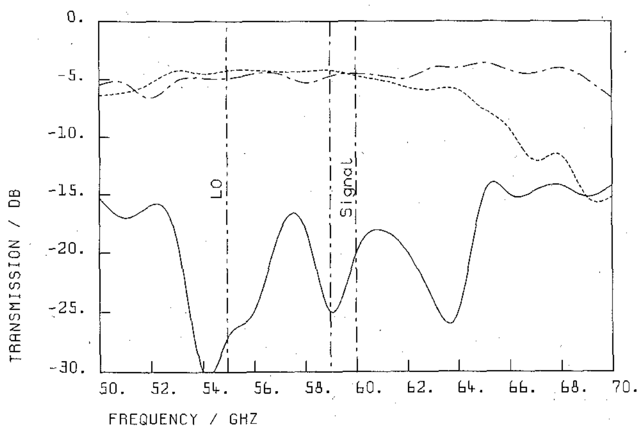

Fig. 9. Measured characteristics of the branch-line coupler.

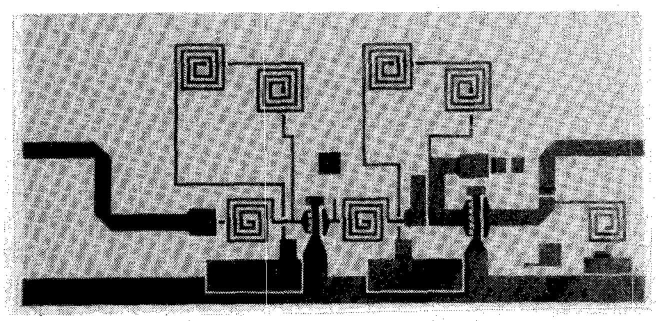

Fig. 11. IF amplifier chip.

on the basis of the magnetic wall waveguide model [12]. With this model S parameters of these structures can be calculated as a function of frequency and geometrical dimensions. LO at 55.4 GHz and signal frequencies at 60 GHz are fed to the diodes through a branch-line coupler which has been designed using this software taking into account improved models of the MSL tee junction and coupling between the lines of the coupler. An improved bandwidth of 15 percent was achieved by adding four open-ended stubs to the coupler [13].

Fig. 9 shows the characteristic of a separately fabricated coupler measured in a V-band test fixture. The coupling is approximately 4 dB in the frequency range of operation.

Two side-coupled dc stops allow dc bias of the diodes through two band-stop filters for optimum performance. For self-bias operation the two bias pads are grounded. The measured transmission loss of the separately fabricated dc stop is better than 0.6 dB between 50 and 60 GHz compared to 0.5 dB for the calculated value.

A matching network is realized to obtain the optimum performances of the mixer. The matching impedances are optimized for the LO, RF, and image frequencies in order to achieve a good conversion loss for a small LO power. The LO and RF short between the diodes is realized by a radial stub.

Because the coupler has a 90° phase difference between its two output ports, a line length of a quarter wavelength was added to one port to obtain a phase difference of 180° at the center frequency of the mixer. Calculations show that the phase error due to the MSL dispersion within the band of operation is less than $\pm 10°$.

The IF output is also realized as a band-stop filter with a radial stub to reject LO and RF signals. Fig. 10 shows the measured conversion loss and DSB noise figure of the mixer chip versus LO power in self-bias operation. A DSB noise figure of $N_F = 3.3$ dB combined with a 6 dB conversion loss was achieved. The LO power was $P_{LO} = 6.5$ dBm at 55.4 GHz. The IF frequency was 4.1 GHz in this case.

V. IF Amplifier

The IF amplifier was designed for subsequent integration with the mixer described above on a single chip. Fig. 11 shows a photomicrograph of the low-noise amplifier with two stages and parallel resistive feedback at the first stage.

The chip employs two MESFET's with 0.75 μm gate length. The device of the first stage has 12 gate fingers with a total gate width of 600 μm to achieve a low gate resistance and with it a low device noise figure. The device of the second stage has eight gate fingers with a total gate width of 400 μm. An equivalent circuit with 12 elements of both devices is shown in Fig. 12. The element values were derived from scattering parameter measurements with a microstrip test fixture up to 6 GHz.

The resistive feedback at the first stage made it possible to obtain unconditional stability and the desired bandwidth of approximately 1 GHz. In order to meet these

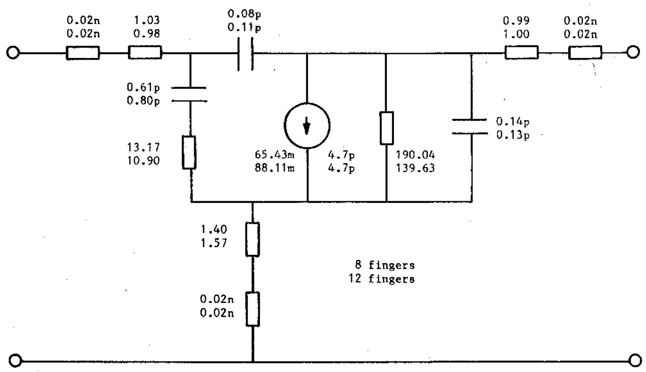

Fig. 12. Equivalent circuits of the MESFET's in the IF amplifier.

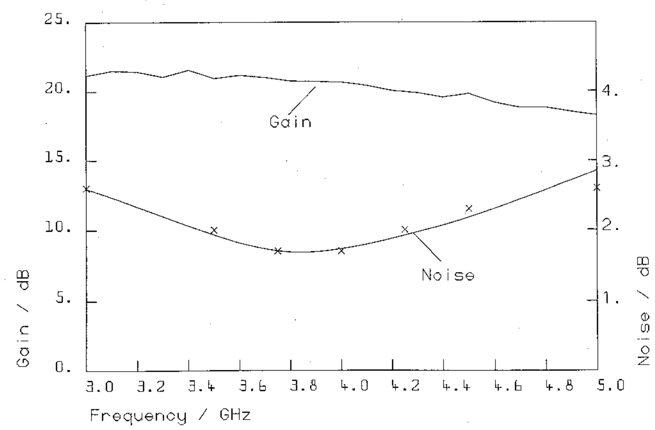

Fig. 13. Noise figure and associated gain of the IF amplifier.

conditions on the one hand, but also to retain a low noise figure for the first stage on the other, a value of 2000 Ω for the feedback resistor was chosen [14]. The optimum reflection coefficient of the first stage for minimum noise figure was determined from the measured noise parameters (minimum noise figure, equivalent noise resistance, optimum reflection coefficient) and scattering parameters of the first MESFET device and the element values of the feedback network [15].

For minimum noise figure a network consisting of a series capacitance and a shunt inductance with a block capacitance transformed the input impedance of 50 Ω into the required optimum reflection coefficient. The matching between the output impedance of the first stage and the input impedance of the second-stage MESFET, and between the output impedance of the second-stage MESFET and the 50 Ω output impedance, respectively, was obtained by a series inductance. The on-chip bias circuit consisted of a 2000 Ω series resistance for each gate and two series inductances and a shunt capacitance for each drain.

Resistors, capacitors, and inductors were realized by epitaxial layer resistors, MIM capacitors, and square spiral inductors. The dimensions of the elements are determined from equivalent circuits, which were derived from the measured scattering parameters of various elements with different dimensions. Since square spiral inductors have a rather low resonance frequency, caused by the low substrate thickness, two series inductors instead of one are used in the drain bias networks.

Fig. 13 contains the measured results for the noise figure and associated gain of the fabricated amplifier. The minimum noise figure was 1.7 dB with an associated gain of 20.6 dB at 4 GHz.

VI. Conclusion

A GaAs technology using a combination of implantation and MOCVD has been developed which allows the fabrication of Schottky mixer diodes and MESFET's on a single chip. A 60 GHz single balanced mixer and an IF amplifier have been made using this technology and can be integrated in a receiver chip [16]. The mixer has a conversion loss of 6 dB and a minimum noise figure of 3.3 dB. With the IF amplifier a gain of 20.6 dB combined with a minimum noise figure of 1.7 dB at 4 GHz has been achieved. Using these data, an overall gain of about 14 dB and a noise figure of nearly 6 dB (DSB) can be expected.

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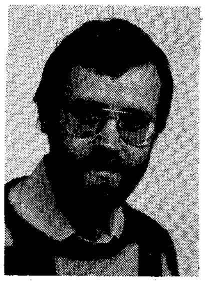

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